

WHAT IS CLAIMED IS:

1 . An XY-addressing type solid-state imaging apparatus comprising:

a plurality of pixels arranged in a two-dimensional matrix; and

a horizontal scanning circuit and a vertical scanning circuit for reading signals of the pixels;

wherein said vertical scanning circuit concurrently selects the pixels of  $n$  rows ( $n$  being an integer of 2 or more) at a first timing to concurrently effect a reset operation of the pixels of the  $n$  rows thereof and selects at a second timing subsequent to the first timing the pixels of  $n$  rows of the address different from the rows selected at the first timing to effect a reset operation of the pixels of the  $n$  rows thereof, reset operation in this manner being repeated to effect a reset operation of all pixels.

2 . The solid-state imaging apparatus according to claim 1, wherein said pixels of the  $n$  rows concurrently selected for the reset operation to be effected are the pixels of the rows having consecutive addresses.

3 . The solid-state imaging apparatus according to claim 1, wherein said pixels of the  $n$  rows concurrently selected

for the reset operation to be effected are the pixels of the rows having discrete addresses.

4 . The solid-state imaging apparatus according to any one of claims 1 to 3, wherein said vertical scanning circuit comprises: a row selecting section; and a timing pulse generating section to which output signals of the row selecting section and timing signals are inputted to generate control signals for effecting pixel operation.

5 . The solid-state imaging apparatus according to claim 4, wherein said row selecting section comprises a decoder.

6 . The solid-state imaging apparatus according to claim 4, wherein said row selecting section comprises a shift register.

7 . The solid state imaging apparatus according to claim 4, wherein said timing pulse generating section comprises a logic circuit.

8 . The solid state imaging apparatus according to claim 5, wherein said timing pulse generating section comprises a logic circuit.

9 .      The solid state imaging apparatus according to claim 6, wherein said timing pulse generating section comprises a logic circuit.